In the claims

1. (currently amended) A method for fabricating a semiconductor device comprising:

forming a gate oxide and a gate electrode on a semiconductor substrate;

performing a first ion implantation process for the formation of a (lightly doped drain) LDD region in the substrate;

forming spacers on the sidewalls of the gate electrode;

performing a second ion implantation process for the formation of a junction region in the substrate using the spacers as a mask;

forming a trench for device isolation by removing selectively the top portion of the substrate between the spacers;

forming ~~a sidewall oxide~~ an oxidation layer on the ~~resulting~~ whole substrate except on the spacers;

forming a diffusion barrier on the ~~sidewall oxide~~ layer resulting substrate;

depositing a gap filling insulation layer over the diffusion barrier;

planarizing the gap filling insulating layer; and

removing selectively some part of the gap filling insulation layer to form contact holes.

2. (original) A method as defined by claim 1, wherein the gap filling insulation layer is formed of boro-phosphosilicate glass (BPSG).

3. (original) A method as defined by claim 1, wherein the diffusion barrier is formed of amorphous silicon.

4. (original) A method as defined by claim 1, wherein the diffusion barrier is an N-doped oxide layer.

5. (original) A method as defined by claim 1, wherein the gap filling insulation layer is formed of undoped silicate glass (USG).

6. (original) A method as defined by claim 1, wherein the gap filling insulation layer is used as both a device isolation layer and an interlayer insulation layer.